

RESPONSE TO ELECTION/RESTRICTION AND  
AMENDMENT UNDER 37 C.F.R. § 1.111  
U.S. Application No. 09/864,259  
Attorney Docket: Q62964

**REMARKS**

This Response to Election/Restriction and Amendment under 37 C.F.R. § 1.111 supplements the Amendment filed on September 26, 2002 in response to the office Action of May 6, 2002, and also responds to the Examiner's communication of December 16, 2002, in which the Examiner indicates that he did not enter the Amendment filed on September 26, 2002, alleging that new claims 23-30 were not directed to the elected species.

The Examiner has withdrawn claims 23-30 from consideration as being drawn to a non-elected invention. Applicant respectfully traverses the Examiner's constructive election and withdrawal of claims 23-30, and Applicant adds new claims 31-38, which are clearly directed to and readable on the elected species. Independent claims 31 and 32 are generic, and claims 23-30 are a species of generic claims 31 and 32.

Applicant submits that allowance of the generic claims should result in the allowance of the respective specie claims. Therefore, upon allowance of generic claims 31 and 32, Applicant submits that claims 23-30 should be allowed at least by virtue of being a species of the allowed generic claims. In addition, dependent claims 33-34 and 35-38 should be allowable at least by virtue of their dependence on base claims 31 and 32, respectively.

In addition, Applicant respectfully submits that claims 23-38 patentably distinguish over the prior art. The present invention relates to a method of manufacturing a semiconductor memory device having more than one memory cell so as to prevent the formation of a metal

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silicide layer on a diffusion layer that is common to two adjacent memory cells. The prior art cited by the Examiner relates to a different device entirely.

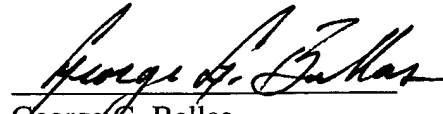
Specifically, U.S. Patent 6,339,237 to Nomachi et al. does not disclose or suggest the present claimed invention. For example, the diffusion layer 18a in the region A shown in Fig. 15 of Nomachi can be used only for one memory cell as a result of the formation of the insulating layer 14 on the left side of the diffusion layer 18a. Insulating layer 14 insulates the conductive layer 16a so that it cannot operate as a gate for a transistor that has the diffusion layer 18a as its source or drain region. The diffusion layer 18a can be used only as source (or drain) region of the single memory cell transistor that has the conductive layer 16b as its gate and another diffusion layer 18b as the drain (or source) region. Therefore, the device structure relating to the layer 18a of Nomachi teaches away from the present invention, which requires a diffusion layer that is common to two adjacent memory cells.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,

  
George G. Ballas  
Registration No. P-52,587

SUGHRUE MION, PLLC  
Telephone: (202) 293-7060  
Facsimile: (202) 293-7860

WASHINGTON OFFICE



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Date: February 19, 2003

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**APPENDIX**

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

Claims 31-38 are added as new claims.